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ELEC 2210 – T 11:00

Experiment #9 MOSFETS and CMOS Inverter

03/16/2021

**Introduction:**

The goal of this lab was to practice using PMOS and NMOS transistors to better understand their I-V curves how to construct them as CMOS inverters. Students used ALD1105 chip to accomplish these goals. Information and experiences gained in this lab will help students better understand MOSFETS and CMOS inverter logic.

**Step 1.1 and 1.2: NMOS/PMOS IDS-VDS and IDS-VGS Characteristics**

Using the diagram from the lab manual, a circuit was constructed using the ALD1105 CMOS chip and the RC4558 operational amplifier. The IDS-VDS and IDS-VGS characteristics for NMOS were obtained using the LabView program and can be seen below. From this data, the first order theory can be verified and VDsat can be acquired. After getting this data, the Vtn is ~ 1V.

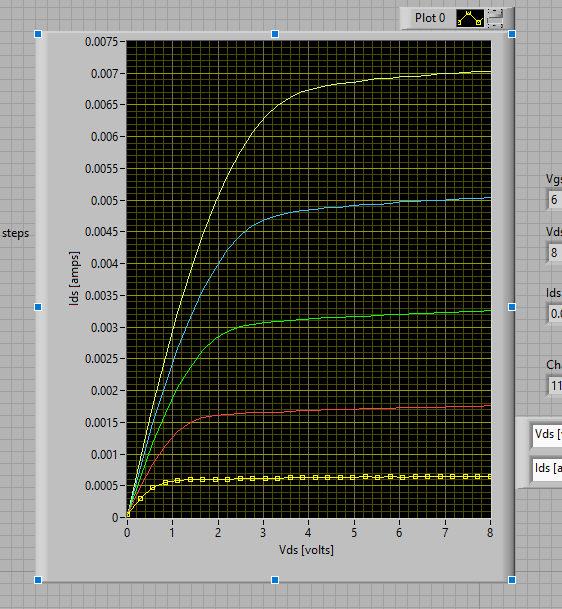


Figure 1: NMOS IDS-VDS Characteristics

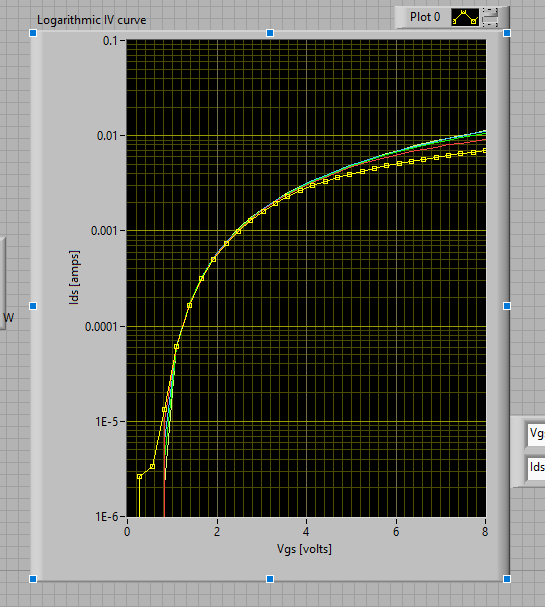
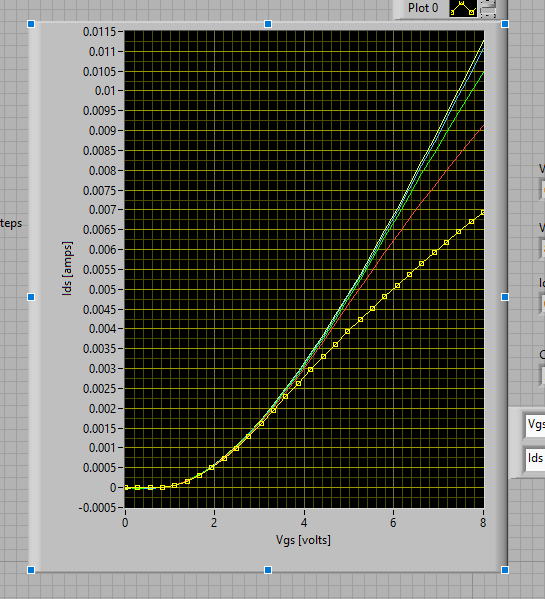


Figure 2: PMOS IDS-VGS Characteristics

|  |  |  |
| --- | --- | --- |
| **Vgs** | **VDsat** | **Idsat** |
| 2 | 1V | 0.5mA |
| 3 | 2V | 1.6mA |
| 4 | 3V | 3.1mA |
| 5 | 4V | 4.7mA |
| 6 | 5V | 6.7mA |

Table 1: VDsat Calculations

**Step 2.1 and 2.2: PMOS IDS-VDS and IDS-VGS Characteristics**

Using the diagram from the lab manual, a circuit was constructed using the ALD1105 CMOS chip and the RC4558 operational amplifier. The IDS-VDS and IDS-VGS characteristics for PMOS were obtained using the LabView program and can be seen below. From this data, the first order theory can be verified and VDsat can be acquired. After getting this data, the Vtn is ~ 1V.

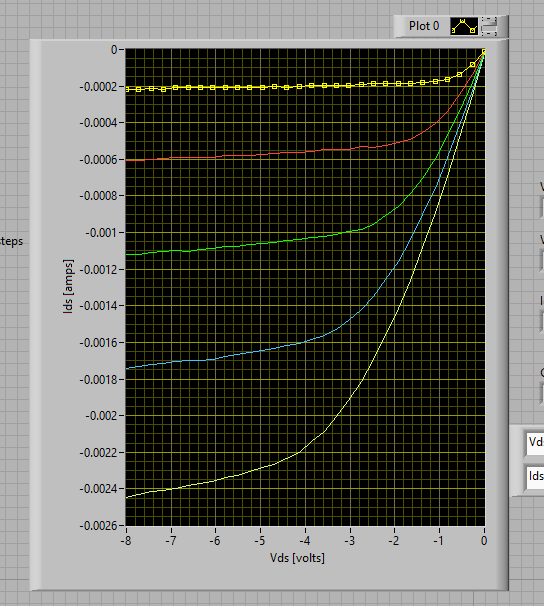


Figure 3: PMOS IDS-VDS Characteristics

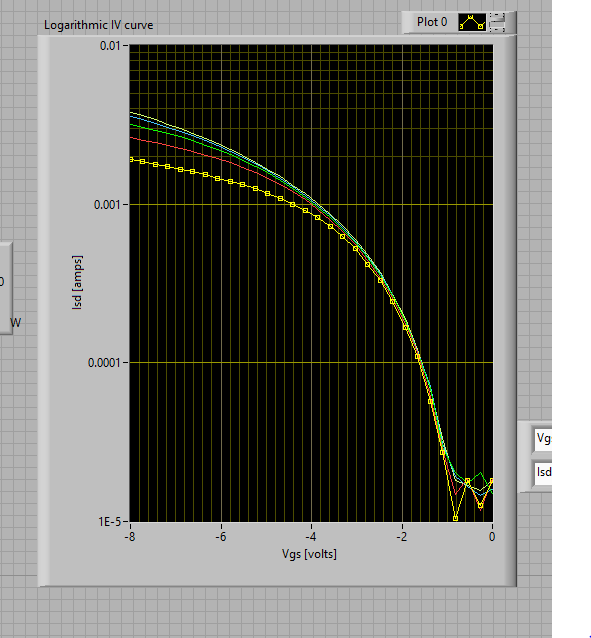
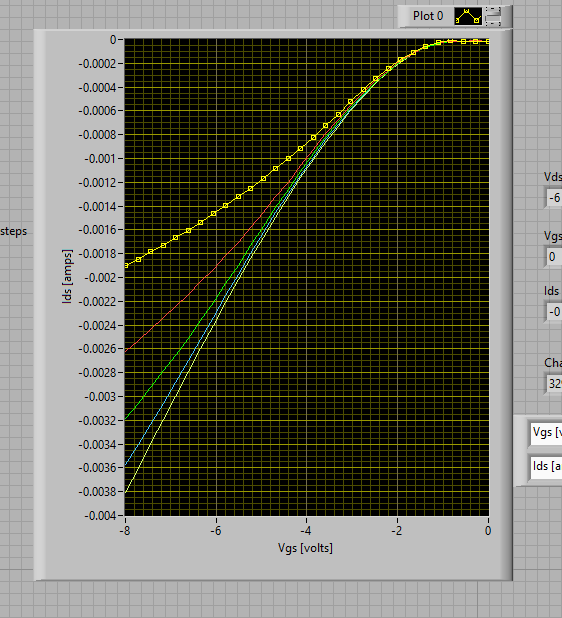


Figure 4: PMOS IDS-VGS Characteristics

|  |  |  |
| --- | --- | --- |
| **Vgs** | **VDsat** | **Idsat** |
| -2 | -1V | -0.2mA |
| -3 | -2V | -0.55mA |
| -4 | -3V | -1.0mA |
| -5 | -4V | -1.6mA |
| -6 | -5V | -2.3mA |

Table 2: Table 1: VDsat Calculations

**Step 3: CMOS Inverter**

Using the diagram from the lab manual, the ALD1105 chip was used to construct a CMOS inverter. Then, using the function generator and the variable power supplies, the frequency and VDD values were varied to see their effects on the graph. The delay of the inverter will be shortened by increasing VDD.

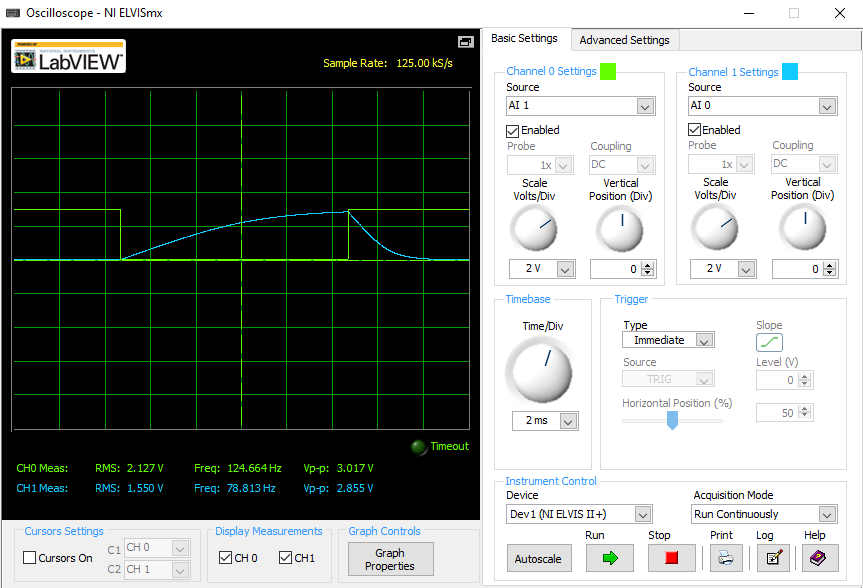


Figure 5: CMOS Inverter 50 Hz VDD=3V

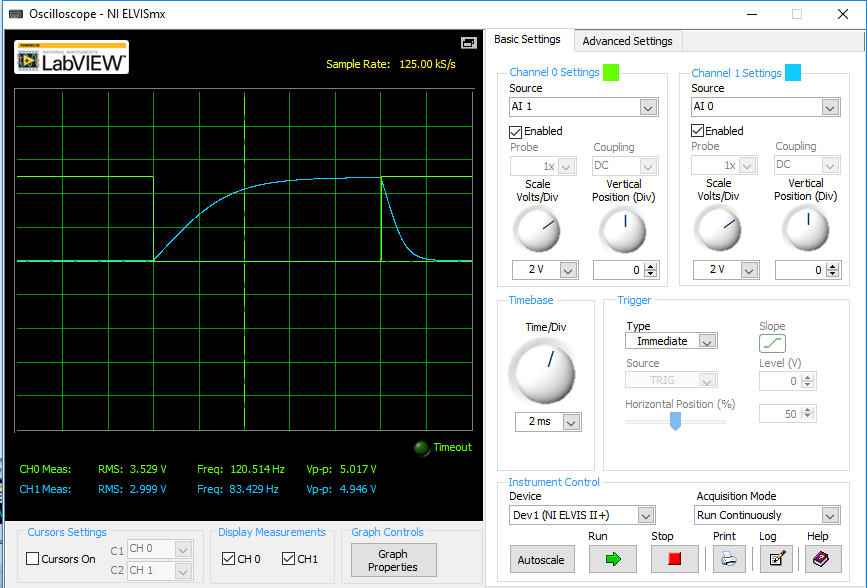


Figure 6: CMOS Inverter 50 Hz VDD=5V

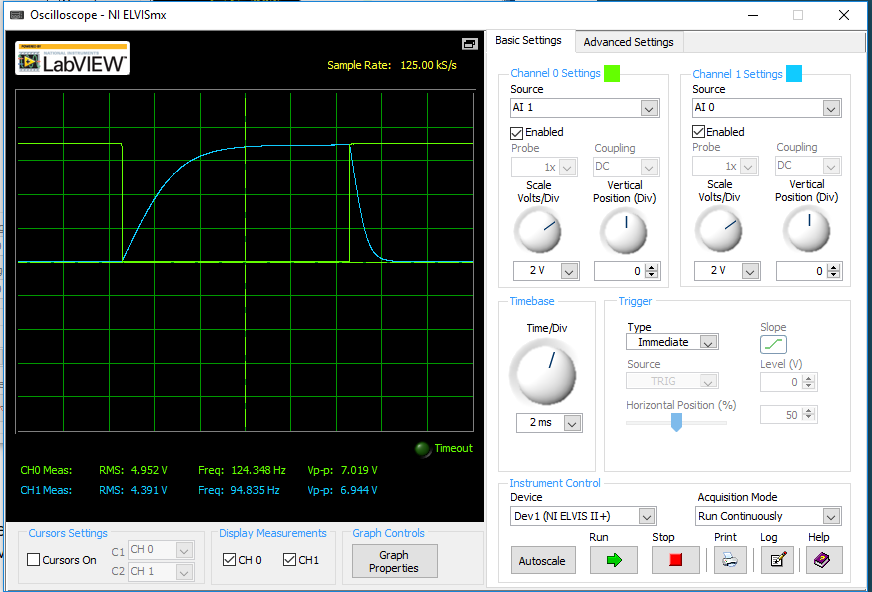


Figure 7: CMOS Inverter 50 Hz VDD=7V

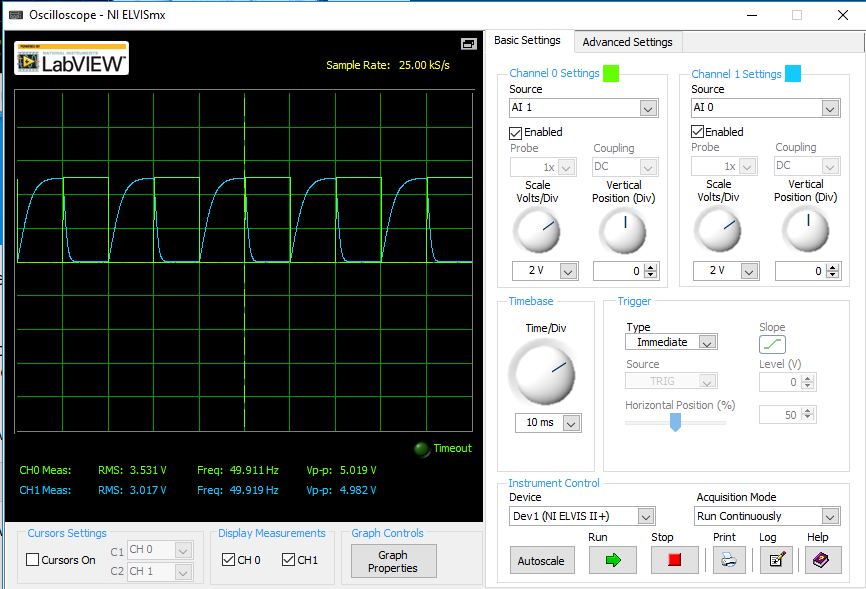


Figure 8: CMOS Inverter 10 Hz VDD=5V

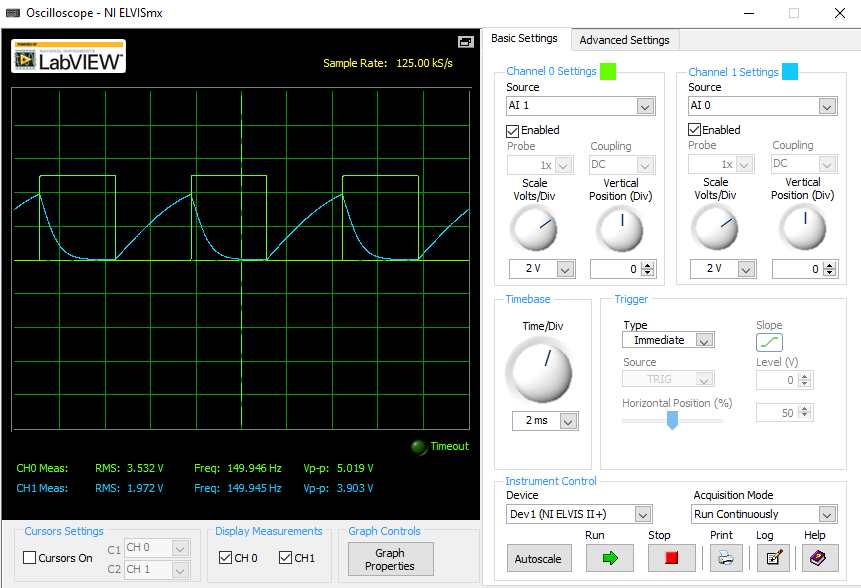


Figure 9: CMOS Inverter 150 Hz VDD=5V

**Step 4: CMOS Inverter Voltage Transfer Curve**

In this step, the voltage transfer curve of the inverter will be measured. The same circuit from Step 3 was used, except the capacitor was removed and the AO0 lead was moved to the inverter input instead of the function generator. The inverter switches logic values around 1.9V. This is because PMOS and NMOS transistors are not symmetric on ICs.

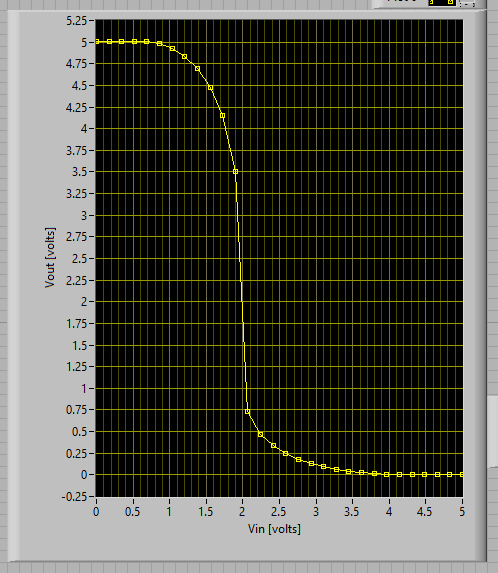


Figure 10: CMOS Voltage Transfer Curve

**Conclusion:**

This lab provided me with a better understanding of MOSFETs and CMOS inverters. The lab did a good job showing and explaining how the current behaves in the transistors. I particularly enjoyed the bonus and being able to wire up the oscillator. That part was more challenging than the rest of the lab. I seemed to have run into a few problems with the parts, but after handling that things become much easier. Other than that, I was able to complete the lab with no issues.

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